WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, including a dynamic random access memory (DRAM) unit, the DRAM unit comprising:

a plurality of bit line pairs, each bit line pair including a first bit line and a second bit line;

a plurality of activatable word lines, at most one word line being activated at a time;

a plurality of memory cells; and

a plurality of multiplexers,

the first bit line and the second bit line within each bit line pair being aligned with each other in an end-to-end arrangement; and

the first bit lines being arranged substantially in parallel with each other and consecutively adjacent to one another; and

the second bit lines being arranged substantially in parallel with each other and consecutively adjacent to one another; and

each word line being associated with either all of the first bit lines or all of the second bit lines, such that a first array is formed by the first bit lines and their associated word lines and a second array is formed by the second bit lines and their associated word lines; and

one of the plurality of memory cells being associated with every other bit line along each word line, such that for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are each associated with one of the plurality of memory cells; and

each of the plurality of multiplexers being in communication with a voltage source input and with two adjacent bit lines within one of the two arrays; and

wherein when a word line is activated, each of the plurality of multiplexers is configured to output a difference between signal levels of the two adjacent bit lines in communication with that multiplexer.

2. The device of claim 1, the array to which the activated word line belongs acting as a sense array, and the array to which the activated word line does not belong acting as a reference array, and the DRAM unit further comprising an activatable dummy word line in the first array and an activatable dummy word line in the second array, and the device being configured to detect signal levels in a common mode by activating the dummy word line in the reference array and detecting a signal level of the activated word line differentially as compared to a signal level of the activated dummy word line.

3. The device of claim 2, the DRAM unit further comprising two interconnect layers, including a first interconnect layer and a second interconnect layer, and each bit line being associated with both interconnect layers.

4. The device of claim 3, the first interconnect layer comprising a first metal layer, and the second interconnect layer comprising a second metal layer.

5. The device of claim 3, the first interconnect layer comprising a metal layer, and the second interconnect layer comprising a polysilicon layer.

6. The device of claim 3, the first interconnect layer comprising a first polysilicon layer, and the second interconnect layer comprising a second polysilicon layer.

7. The device of claim 2, the DRAM unit being manufactured using a logic process.

8. The device of claim 2, the DRAM unit being manufactured using a DRAM process.

9. A semiconductor integrated circuit device, including a dynamic random access memory (DRAM) unit, the DRAM unit comprising:

a plurality of bit line pairs, each bit line pair including a first bit line and a second bit line;

a plurality of activatable word lines, at most one word line being activated at a time;

a plurality of memory cells;

a plurality of multiplexers; and

a first interconnect layer and a second interconnect layer,

the first bit line and the second bit line within each bit line pair being adjacent to each other; and

each bit line being associated with both interconnect layers; and

each word line being associated with all of the bit lines, such that an array is formed by the bit lines and the associated word lines; and

one of the plurality of memory cells being associated with every other bit line along each word line, such that for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are each associated with one of the plurality of memory cells; and

each of the plurality of multiplexers being in communication with a voltage source input and with a first bit line and a second bit line within a bit line pair; and

wherein when a word line is activated, each of the plurality of multiplexers is configured to output a difference between signal levels of the two adjacent bit lines in communication with that multiplexer.

10. The device of claim 9, the DRAM unit further comprising an activatable dummy word line, and the device being configured to detect signal levels in a common mode by activating the dummy word line and detecting a signal level of the activated word line differentially as compared to a signal level of the activated dummy word line.

11. The device of claim 10, the first interconnect layer comprising a first metal layer, and the second interconnect layer comprising a second metal layer.

12. The device of claim 11, the first bit line and the second bit line within each bit line pair being twisted at at least one point such that half of each bit line is associated with the first metal layer and half of each bit line is associated with the second metal layer.

13. The device of claim 12, the first bit line and the second bit line within at least one bit line pair being twisted at at least two points such that half of each bit line is associated with the first metal layer and half of each bit line is associated with the second metal layer.

14. The device of claim 10, the first interconnect layer comprising a metal layer, and the second interconnect layer comprising a polysilicon layer.

15. The device of claim 10, the first interconnect layer comprising a first polysilicon layer, and the second interconnect layer comprising a second polysilicon layer.

16. The device of claim 10, the DRAM unit being manufactured using a logic process.

17. The device of claim 10, the DRAM unit being manufactured using a DRAM process.

18. A semiconductor integrated circuit device, including a dynamic random access memory (DRAM) unit, the DRAM unit including a substrate and a plurality of memory cells, each memory cell comprising:

a transistor, including a gate, the gate comprising polysilicon;

a gate oxide arranged between the gate and the substrate;

a cell plate, the cell plate comprising one of polysilicon and a metal conductor, and the cell plate being physically isolated from the gate by a minimum displacement; and

a dielectric material arranged between the cell plate from the substrate, the dielectric material having a high dielectric constant,

wherein a direction of the minimum displacement is substantially orthogonal to the substrate such that a component of the minimum displacement parallel to the substrate is substantially zero.

19. The device of claim 18, the dielectric material comprising tantalum oxide.

20. The device of claim 18, the dielectric material comprising aluminum oxide.

21. The device of claim 18, the dielectric material comprising oxinitride.

22. The device of claim 18, the DRAM unit being manufactured using a logic process.

23. The device of claim 18, the DRAM unit being manufactured using a DRAM process.

24. A semiconductor integrated circuit device, including a dynamic random access memory (DRAM) unit, the DRAM unit including a substrate and a plurality of memory cells, each memory cell comprising:

a transistor, including a gate, the gate comprising polysilicon;

a gate oxide arranged between the gate and the substrate;

a cell plate, the cell plate comprising one of polysilicon and a metal conductor, and the cell plate being physically isolated from the gate; and

a dielectric material arranged between the cell plate and the substrate, the dielectric material having a high dielectric constant,

wherein the cell plate and the gate are physically located on different vertical levels as seen from the substrate.

25. The device of claim 24, the dielectric material comprising tantalum oxide.

26. The device of claim 24, the dielectric material comprising aluminum oxide.

27. The device of claim 24, the dielectric material comprising oxinitride.

28. The device of claim 24, the DRAM unit being manufactured using a logic process.

29. The device of claim 24, the DRAM unit being manufactured using a DRAM process.

30. An apparatus for reducing noise and overall bit line capacitance in a DRAM device, comprising:

a plurality of pairs of bit line means for conducting electrical signals, each pair including a first bit line means and a second bit line means;

a plurality of activatable word line means for conducting electrical signals, at most one word line means being activated at a time;

a plurality of means for storing data; and

a plurality of means for multiplexing,

the first bit line means and the second bit line means within each bit line pair being aligned with each other in an end-to-end arrangement; and

the first bit line means being arranged substantially in parallel with each other and consecutively adjacent to one another; and

the second bit line means being arranged substantially in parallel with each other and consecutively adjacent to one another; and

each word line means being associated with either all of the first bit line means or all of the second bit line means, such that a first array is formed by the first bit line means and their associated word line means and a second array is formed by the second bit line means and their associated word line means; and

one of the plurality of means for storing data being associated with every other bit line means along each word line means, such that for each word line means, each bit line means that is not associated with one of the plurality of means for storing data acts as a shield between bit line means that are each associated with one of the plurality of means for storing data; and

each of the plurality of means for multiplexing being in communication with a voltage source input and with two adjacent bit line means within one of the two arrays; and

wherein when a word line means is activated, each of the plurality of means for multiplexing is configured to output a difference between signal levels of the two adjacent bit line means in communication with that means for multiplexing.

31. The apparatus of claim 30, the array to which the activated word line means belongs acting as a sense array, and the array to which the activated word line means does not belong acting as a reference array, and the apparatus further comprising:

an activatable dummy word line means for conducting electrical signals in the first array;

an activatable dummy word line means for conducting electrical signals in the second array; and

means for detecting signal levels in a common mode by activating the dummy word line means in the reference array and detecting a signal level of the activated word line means differentially as compared to a signal level of the activated dummy word line means.

32. The apparatus of claim 31, the device further comprising two interconnect layers, including a first interconnect layer and a second interconnect layer, and each bit line means being associated with both interconnect layers.

33. The apparatus of claim 32, the first interconnect layer comprising a first metal layer, and the second interconnect layer comprising a second metal layer.

34. The apparatus of claim 32, the first interconnect layer comprising a metal layer, and the second interconnect layer comprising a polysilicon layer.

35. The apparatus of claim 32, the first interconnect layer comprising a first polysilicon layer, and the second interconnect layer comprising a second polysilicon layer.

36. The apparatus of claim 31, the DRAM device being manufactured using a logic process.

37. The apparatus of claim 31, the DRAM device being manufactured using a DRAM process.

38. An apparatus for reducing noise and overall bit line capacitance in a DRAM device, the device comprising:

a plurality of pairs of bit line means for conducting electrical signals, each pair of bit line means including a first bit line means and a second bit line means;

a plurality of activatable word line means for conducting electrical signals, at most one word line means being activated at a time;

a plurality of means for storing data;

a plurality of means for multiplexing; and

a first interconnect layer and a second interconnect layer,

each bit line means being associated with both interconnect layers;

the first bit line means and the second bit line means within each pair of bit line means being arranged to be adjacent to each other;

each word line means being associated with all of the bit line means, such that an array is formed by the bit line means and the associated word line means;

one of the plurality of means for storing data being associated with every other bit line means along each word line means, such that for each word line means, each bit line means that is not associated with one of the plurality of means for storing data acts as a shield

between bit line means that are each associated with one of the plurality of means for storing data; and

each of the plurality of means for multiplexing being in communication with a voltage source and with a first bit line means and a second bit line means within a pair of bit line means,

wherein when a word line means is activated, each of the plurality of means for multiplexing is configured to output a difference between signal levels of the two adjacent bit line means in communication with that means for multiplexing.

39. The apparatus of claim 38, the apparatus further comprising:

an activatable dummy word line means for conducting electrical signals; and

means for detecting signal levels in a common mode by activating the dummy word line means and detecting a signal level of the activated word line means differentially as compared to a signal level of the activated dummy word line means.

40. The apparatus of claim 39, the first interconnect layer comprising a first metal layer, and the second interconnect layer comprising a second metal layer.

41. The apparatus of claim 40, further comprising means for twisting the first bit line means and the second bit line means within each pair of bit line means at at least one point such that half of each bit line means is associated with the first metal layer and half of each bit line means is associated with the second metal layer.

42. The apparatus of claim 41, further comprising means for twisting the first bit line means and the second bit line means within at least one pair of bit line means at at least two points

such that half of each bit line means is associated with the first metal layer and half of each bit line means is associated with the second metal layer.

43. The apparatus of claim 39, the first interconnect layer comprising a metal layer, and the second interconnect layer comprising a polysilicon layer.

44. The apparatus of claim 39, the first interconnect layer comprising a first polysilicon layer, and the second interconnect layer comprising a second polysilicon layer.

45. The apparatus of claim 39, the DRAM device being manufactured using a logic process.

46. The apparatus of claim 39, the DRAM device being manufactured using a DRAM process.

47. An apparatus for reducing area in a DRAM device, the DRAM device including a substrate means and a plurality of means for storing data, each means for storing data comprising:

a transistor means for switching, including a gate means, the gate means comprising polysilicon;

gate insulating means for insulating the gate means from the substrate means;

a cell plate means for providing an electric field, the cell plate means comprising one of polysilicon and a metal conductor, and the cell plate means being physically isolated from the gate means by a minimum displacement to prevent short circuits; and

a dielectric means for separating the cell plate means from the substrate means, the dielectric means having a high dielectric constant,

wherein a direction of the minimum displacement is substantially orthogonal to the substrate means, such that a component of the minimum displacement parallel to the substrate means is substantially zero.

48. The apparatus of claim 47, the dielectric means comprising tantalum oxide.

49. The apparatus of claim 47, the dielectric means comprising aluminum oxide.

50. The apparatus of claim 47, the dielectric means comprising oxinitride.

51. The apparatus of claim 47, the DRAM device being manufactured using a logic process.

52. The apparatus of claim 47, the DRAM device being manufactured using a DRAM process.

53. An apparatus for reducing area in a DRAM device, the DRAM device including a substrate means and a plurality of means for storing data, each means for storing data comprising:

a transistor means for switching, including a gate means, the gate means comprising polysilicon;

gate insulating means for insulating the gate means from the substrate means;

a cell plate means for providing an electric field, the cell plate means comprising one of polysilicon and a metal conductor, and the gate means being physically located on a first vertical level as seen from the substrate means and the cell plate means being physically located on a second vertical level as seen from the substrate means; and

a dielectric means for separating the cell plate means from the substrate means, the dielectric means having a high dielectric constant.

54. The apparatus of claim 53, the dielectric means comprising tantalum oxide.

55. The apparatus of claim 53, the dielectric means comprising aluminum oxide.

56. The apparatus of claim 53, the dielectric means comprising oxinitride.

57. The apparatus of claim 53, the DRAM device being manufactured using a logic process.

58. The apparatus of claim 53, the DRAM device being manufactured using a DRAM process.

59. A method of reducing noise and overall bit line capacitance in a DRAM device, the device including a plurality of bit line pairs, a plurality of activatable word lines, a plurality of memory cells, and a plurality of multiplexers, each bit line pair including a first bit line and a second bit line, and at most one word line being activated at a time, the method comprising the steps of:

aligning the first bit line and the second bit line within each bit line pair in an end-to-end arrangement;

arranging the first bit lines substantially in parallel with each other and consecutively adjacent to one another;

arranging the second bit lines substantially in parallel with each other and consecutively adjacent to one another;

associating each word line with either all of the first bit line means or all of the second bit line means, such that a first array is formed by the first bit lines and their associated word lines and a second array is formed by the second bit lines and their associated word lines;

associating one of the plurality of memory cells with every other bit line along each word line, such that for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are each associated with one of the plurality of memory cells;

bringing each multiplexer of the plurality of multiplexers into communication with a voltage source input and with two adjacent bit lines within one of the two arrays; and

configuring each multiplexer to output a difference between signal levels of the two adjacent bit lines in communication with that multiplexer when a word line is activated.

60. The method of claim 59, the array to which the activated word line belongs acting as a sense array, and the array to which the activated word line does not belong acting as a reference array, and the device further including an activatable dummy word line in the first array and an activatable dummy word line in the second array, and the method further comprising the step of detecting signal levels in a common mode by activating the dummy word line in the reference array and detecting a signal level of the activated word line differentially as compared to a signal level of the activated dummy word line.

61. The method of claim 60, the device further comprising two interconnect layers, including a first interconnect layer and a second interconnect layer, and the method further comprising the step of associating each bit line with both interconnect layers.

62. The method of claim 61, the first interconnect layer comprising a first metal layer, and the second interconnect layer comprising a second metal layer.

63. The method of claim 61, the first interconnect layer comprising a metal layer, and the second interconnect layer comprising a polysilicon layer.

64. The method of claim 61, the first interconnect layer comprising a first polysilicon layer, and the second interconnect layer comprising a second polysilicon layer.

65. The method of claim 60, the DRAM device being manufactured using a logic process.

66. The method of claim 60, the DRAM device being manufactured using a DRAM process.

67. A method of reducing noise and overall bit line capacitance in a DRAM device, the device including a plurality of bit line pairs, a plurality of activatable word lines, a plurality of memory cells, a plurality of multiplexers, and a first interconnect layer and a second interconnect layer, each bit line pair including a first bit line and a second bit line, and at most one word line being activated at a time, the method comprising the steps of:

associating each bit line with both interconnect layers;

arranging the first bit line and the second bit line within each bit line pair to be adjacent to each other;

associating each word line with all of the bit lines, such that an array is formed by the bit lines and the associated word lines;

associating one of the plurality of memory cells with every other bit line along each word line, such that for each word line, each bit line that is not associated with one of the

plurality of memory cells acts as a shield between bit lines that are each associated with one of the plurality of memory cells;

bringing each multiplexer of the plurality of multiplexers into communication with a voltage source and with a first bit line and a second bit line within a bit line pair; and

configuring each multiplexer to output a difference between signal levels of the two adjacent bit lines in communication with that multiplexer when a word line is activated.

68. The method of claim 67, the device further including an activatable dummy word line, and the method further comprising the step of detecting signal levels in a common mode by activating the dummy word line and detecting a signal level of the activated word line differentially as compared to a signal level of the activated dummy word line.

69. The method of claim 68, the first interconnect layer comprising a first metal layer, and the second interconnect layer comprising a second metal layer.

70. The method of claim 69, further comprising the step of twisting the first bit line and the second bit line within each bit line pair at at least one point such that half of each bit line is associated with the first metal layer and half of each bit line is associated with the second metal layer.

71. The method of claim 70, further comprising the step of twisting the first bit line and the second bit line within at least one bit line pair at at least two points such that half of each bit line is associated with the first metal layer and half of each bit line is associated with the second metal layer.

72. The method of claim 68, the first interconnect layer comprising a metal layer, and the second interconnect layer comprising a polysilicon layer.

73. The method of claim 68, the first interconnect layer comprising a first polysilicon layer, and the second interconnect layer comprising a second polysilicon layer.

74. The method of claim 68, the DRAM device being manufactured using a logic process.

75. The method of claim 68, the DRAM device being manufactured using a DRAM process.

76. A method of reducing area in a DRAM device, the DRAM device including a substrate and a plurality of memory cells, each memory cell including a transistor having a gate comprising polysilicon and a cell plate, the method comprising the steps of:

arranging a gate oxide between the gate and the substrate;

physically isolating the cell plate from the gate by a minimum displacement to prevent short circuits; and

arranging a dielectric material having a high dielectric constant between the cell plate and the substrate,

wherein a direction of the minimum displacement is substantially orthogonal to the substrate, such that a component of the minimum displacement parallel to the substrate is substantially zero.

77. The method of claim 76, the dielectric material comprising tantalum oxide.

78. The method of claim 76, the dielectric material comprising aluminum oxide.

79. The method of claim 76, the dielectric material comprising oxinitride.

80. The method of claim 76, the DRAM device being manufactured using a logic process.

81. The method of claim 76, the DRAM device being manufactured using a DRAM process.

82. A method of reducing area in a DRAM device, the DRAM device including a substrate and a plurality of memory cells, each memory cell including a transistor having a gate comprising polysilicon and a cell plate, the method comprising the steps of:

arranging a gate oxide between the gate and the substrate;

locating the gate on a first vertical level as seen from the substrate;

locating the cell plate on a second vertical level as seen from the substrate; and

arranging a dielectric material having a high dielectric constant between the cell plate and the substrate.

83. The method of claim 82, the dielectric material comprising tantalum oxide.

84. The method of claim 82, the dielectric material comprising aluminum oxide.

85. The method of claim 82, the dielectric material comprising oxinitride.

86. The method of claim 82, the DRAM device being manufactured using a logic process.

87. The method of claim 82, the DRAM device being manufactured using a DRAM process.